What is claimed is;

1- A semiconductor device comprising:

a substrate having conductive interconnections;

two or more vertically stacked chips on said substrate, each supporting chip having metal standoffs thereon to separate it from the next successive chip; and

a plurality of bond wires connecting at least one chip to said substrate.

2- A semiconductor device as in claim 1, wherein said metal standoffs comprise aluminum islands.

3- A semiconductor device as in claim 1, wherein the thickness of said metal standoffs is 5 to 20 kA.

4- The semiconductor device of claim 1 wherein said standoffs are patterned over the chip passivation layer.

5- The semiconductor device of claim 1 wherein said metal standoffs are thermally conductive.

6- The semiconductor device of claim 1 wherein said metal standoffs are positioned within the area surrounded by bond pads.

7- The semiconductor device of claim 1 wherein a polymeric adhesive secures the first chip to said substrate.

8- The semiconductor device of claim 1 wherein bond wires connect more than one chip to said substrate.

9- The semiconductor device of claim 1 wherein said substrate is a BGA package substrate.

10- The device of claim 1 wherein said metal standoffs have a uniform height.

11- The device of claim 1 wherein said supporting chips include copper bond pads having aluminum caps.

12- A semiconductor chip having one or more metal islands on top of the passivation layer on said chip.

13- The semiconductor chip of claim 12 wherein said islands comprise patterned aluminum.

14- The semiconductor chip of claim 12 wherein said metal islands comprise a thermally conductive material.

15- The semiconductor chip of claim 12 wherein said metal islands are of equal thickness and are within the area surrounded by bond pads.

16- A process for fabricating a semiconductor chip having metal island standoffs, including the steps of:

providing a semiconductor wafer having a plurality of integrated circuit devices covered by a passivation layer having bond pad openings on the top surface;

depositing a layer of metal comprising aluminum on said wafer;

forming a layer of photoresist atop said metal layer;

aligning a mask having patterns for capping bond pads and for adding islands to said wafer;

exposing and developing the photoresist;

etching to remove unwanted metal from the wafer; and

dicing said wafer into individual chips.

17- A process for assembling a semiconductor device having vertically stacked chips with one or more fixed metal standoffs separating said chips including the steps of:

providing a substrate having bonding lands and conductive interconnections;

applying a polymeric chip attach adhesive to said substrate;

aligning a supporting chip having one or more metal standoffs to said adhesive;

applying an adhesive to the islands and area between islands on said supporting chip;

aligning a second chip atop said adhesive on the supporting chip; and

wire bonding each of said chips to said substrate.

18 - The process of claim 17 further including the steps of applying an adhesive to the islands on said second chip, aligning and placing a third chip, curing said adhesive and bonding wires from said third chip to said substrate.